REMARKS

This responds to the Office Action mailed on September 21, 2006.

Claims 7, 10, 12, 14, 18, 21, 27 and 30 are amended, claims 1-6, 11, 16-17 and 26 are canceled, and no claims are added; as a result, claims 7-10, 12-15, 18-25 and 27-32 are now pending in this application.

Applicant reserves all applicable rights not asserted in or with this response, including, for example, the right to rebut tacit and explicit characterizations of the cited reference, and the right to swear behind the cited reference. Applicant makes no admissions regarding the status of any art of record as prior art.

Claim objections

Applicant has amended claim 27 by changing "An article" to "The article", thus the objection to claim 27 is overcome.

§101 Rejection of the Claims

Claims 1-25 were rejected under 35 USC § 101 as being directed to non-statutory matter. Applicant respectfully traverses the rejection for the reasons stated below.

Applicant has canceled claims 1-6, 11, 16-17 and 26, and reproduces amended claim 7 below:

> "A method of software pipelining for improving efficiency of loops handling, the method comprising:
>
> checking for availability of rotating registers to hold computed values that are live across multiple stages in a software-pipelined loop; and
>
> spilling and filling the computed values held in rotating registers in a software-pipelined loop using rotating stack memory locations for rotating registers, when there are no rotating registers available to hold the computed values, wherein the number of the rotating stack memory locations used for spilling and filling the computed values is equal to the number of simultaneous live values generated by the rotating register." (emphasis added to show amendment)

Applicant submits that amended method claim 7 produces a concrete, tangible, and useful result, i.e., improved efficiency of loop handling, by the claimed actions which are to be performed. Additionally, Applicant also submits that amended method claim 7 is directed to a

practical application (i.e., software pipelining). In judging whether a computer-related process is directed to a practical application in the technological arts, what is determinative is not how the computer performs the process, but what the computer does to achieve a practical application. In the method of amended claim 7, the practical application is achieved by the actions of **checking for availability of rotating registers** to hold computed values that are live across multiple stages in a software-pipelined loop; and then **spilling and filling the computed values held in rotating registers** in a software-pipelined loop using rotating stack memory locations for rotating registers, when there are no rotating registers available to hold the computed values.

Therefore, Applicant submits that the method of amended claim 7 is directed to statutory subject matter, and thus for at least the same reason stated for claim 7, methods of claims 8-10, 12-15, and 18-25 are directed to statutory matters. Accordingly, Applicant requests respectfully that the Examiner reconsider and withdraw the §101 rejection of claims 7-10, 12-15, and 18-25.

§112 Rejection of the Claims

Claims 2-3, 21-25, and 30-32 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant respectively traverses the rejection for the reasons stated below.

Applicant has canceled claims 2-3. Applicant has amended claim 21 by changing the limitations "the rotating stack memory locations" in line 6 and "the non-rotating registers" in line 9 to "rotating stack memory locations" and "non-rotating registers" respectively. Applicant has also amended claim 30 by changing the limitation "the rotating stack memory locations" in line 12 to "rotating stack memory locations".

Applicant believes the §112 rejection of claims 21 and 30 is overcome by the amendments, and the §112 rejection of claims 22-25 and 31-32 is also overcome by the amendments because claims 22-25 and 31-32 are dependent upon amended base claim 21 and 30. Accordingly, Applicant requests respectfully that the Examiner reconsider and withdraw the §112 rejection of claims 21-25 and 30-32.

§102 Rejection of the Claims

Claims 1-32 were rejected under 35 USC § 102(e) as being anticipated by Srinivasan (U.S. 6,651,247 B1). Applicant respectfully traverses the rejection for the reasons stated below.

Applicant has canceled claims 1-6, 11, 16-17 and 26, and respectfully submits that Srinivasan does not anticipate claims 7-10, 12-15, 18-25, and 27-32.

"Anticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindermann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 722 F.2d 1452, 220 USPQ 481, 485(Fed. Cir. 1984) (citing Connell v. Sears, Roebuck & Co., 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983))."

Regarding claim 7:

Amended claim 7 recites:

"A method of software pipelining for improving efficiency of loops handling, the method comprising:

checking for availability of rotating registers to hold computed values that are live across multiple stages in a software-pipelined loop;

and spilling and filling the computed values held in rotating registers in a software-pipelined loop using rotating stack memory locations for rotating registers, when there are no rotating registers available to hold the computed values, wherein the number of the rotating stack memory locations used for spilling and filling the computed values is equal to the number of simultaneous live values generated by the rotating register." (emphasis added to show amendments)

In contrast, in column 31, lines 60-65 (relied on by the Office Action), Srinivasan describes, "*The 'targets' of the phi functions are, in the illustrated embodiments of the intermediate representations of FIGD. 7D to 8B, the left hand side operands of the functions; i.e., to the left side of the equal sign. These targets are assigned a rotating register (for example, RRGR1) that has been allocated for the live range associated with the respective phi function.*" However, the cited part of Srinivasan does not teach the feature "**the number of the rotating stack memory locations** used for spilling and filling the computed values is equal to **the number of simultaneous live values generated by the rotating register**" as now recited in amended claim 7, and Applicant cannot find that feature in any other parts of Srinivasan. Thus,

for at least this reason, Applicant submits that Srinivasan does not teach each and every element as claimed in amended claim 7, thus amended claim 7 is not anticipated by Srinivasan.

Regarding claim 10:

Amended claim 10 recites:

"A method of software pipelining for improving efficiency of loops handling, the method comprising:

checking for availability of FP rotating registers to hold FP computed values that are live across multiple stages in a software-pipelined loop; and

spilling and filling the computed values using rotating integer registers for holding addresses of stack memory locations when there are no FP rotating registers available to hold the computed value, the spilling and filling the computed values comprising:

checking for availability of N+1 rotating integer registers, wherein N is number of stages a computed value that needs to be spilled is live in the software-pipelined loop; and

spilling and filling the computed value in stack memory locations whose addresses are held in corresponding N+1 rotating integer registers, when the N+1 rotating integer registers are available." (emphasis added to show amendments)

In contrast, in FIGURE 6, element 530 "Rotating Register Allocator" and col. 2, lines 3-40 relied upon by the Office Action, Applicant cannot find **the branch structure** and the feature "checking for availability of N+1 rotating integer registers, wherein N is number of stages a computed value that needs to be spilled is live in the software-pipelined loop; and spilling and filling the computed value in stack memory locations whose addresses are held in corresponding N+1 rotating integer registers, when the N+1 rotating integer registers are available" as recited in amended claim 10. Thus, for at least this reason, Applicant submits that Srinivasan does not teach each and every element as claimed in amended claim 10, thus amended claim 10 is not anticipated by Srinivasan.

Regarding claim 14:

Amended claim 14 recites:

"A method of software pipelining for improving efficiency of loops handling, the method comprising:

using post-incremented memory operations for spilling and filling of live computed values, held in a FP rotating register, that are live across multiple stages in a software-pipelined

loop, using non-rotating registers, when there are no rotating integer registers available to hold rotating stack memory locations,

checking for availability of N+1 non-rotating integer registers available for spilling and filling, wherein N is a number of stages a computed value that needs to be spilled is live in the software-pipelined loop; and

spilling and filling the computed values in stack memory locations whose addresses are held in corresponding N+1 non-rotating integer registers, when the N+1 non-rotating registers are available." (emphasis added to show amendments)

In contrast, in FIGURE 6 "Rotating Register Allocator" and col. 17, lines 1-5 relied upon by the Office Action, Applicant cannot find **the branch structure** and the feature "checking for availability of N+1 non-rotating integer registers available for spilling and filling, wherein N is a number of stages a computed value that needs to be spilled is live in the software-pipelined loop; and spilling and filling the computed values in stack memory locations whose addresses are held in corresponding N+1 non-rotating integer registers, when the N+1 non-rotating registers are available" as recited in amended claim 14. Thus, for at least this reason, Applicant submits that Srinivasan does not teach each and every element as claimed in amended claim 14, thus amended claim 14 is not anticipated by Srinivasan.

Regarding claim 18:

Amended claim 18 recites:

"A method of software pipelining for improving efficiency of loops handling, the method comprising spilling and filling of live computed values, held in a rotating register, that are live across multiple stages in a software-pipelined loop, using two non-rotating integer registers, when there are no FP rotating registers available and when there are no rotating integer registers available for holding rotating stack memory locations, and when there are not enough non-rotating integer registers available for holding rotating stack memory locations." (emphasis added to show amendments)

In contrast, in FIGURE 5 and col. 32, lines 40-45 relied upon by the Office Action, Applicant cannot find **the branch structure** as recited in amended claim 18. Thus, for at least this reason, Applicant submits that Srinivasan does not teach each and every element as claimed in amended claim 18, thus amended claim 18 is not anticipated by Srinivasan.

Regarding claim 21:

Amended claim 21 recites:

"A method of software pipelining for improving efficiency of loops handling, the method comprising:

checking for availability of rotating integer registers and non-rotating integer registers, to spill and fill computed values held in a FP rotating register, that are live across multiple stages in a software-pipelined loop;

spilling and filling the computed values, held in a FP rotating register, using the rotating integer registers to hold [[the]] rotating stack memory locations, when there are no FP rotating registers available to hold the computed values;

spilling and filling the computed values, held in the FP rotating register, using [[the]] non-rotating registers to hold the rotating stack memory locations, when there are no FP rotating registers to hold the computed values and further when there are no rotating integer registers available for holding rotating stack memory locations; and

spilling and filling the computed values held in the FP rotating register, using two non-rotating integer registers to hold the rotating stack memory locations, when there are no FP rotating registers to hold the computed values, where there are no rotating integer registers available, and further when there are only a few non-rotating integer registers available for holding rotating stack memory locations." (emphasis added to show amendments)

In contrast, in col. 17, lines 1-5; col. 2, lines 30-40; col. 5, lines 5-12 and lines 65-67; and col. 6, lines 1-5 relied upon by the Office Action, Applicant cannot find **the branch structure** as recited in amended claim 21. Thus, for at least this reason, Applicant submits that Srinivasan does not teach each and every element as claimed in amended claim 21, thus amended claim 21 is not anticipated by Srinivasan.

Regarding claim 27:

Amended claim 27 recites:

"[[An]] The article comprising a computer-readable medium which stores computer-executable instructions of claim 26, wherein spilling and filling computed values that are live across multiple stages in a software-pipelined loop using rotating stack memory locations comprises:

checking for availability of rotating integer registers and non-rotating integer registers, to spill and fill computed values held in a FP rotating register, that are live across multiple stages in a software-pipelined loop;

spilling and filling the computed values, held in a FP rotating register, using the rotating integer registers to hold the rotating stack memory locations, when there are no FP rotating registers available to hold the computed values;

spilling and filling the computed values, held in the FP rotating register, using the non-rotating registers to hold the rotating stack memory locations, when there are no FP rotating registers to hold the computed values and further when there are no rotating integer registers available for holding rotating stack memory locations; and

spilling and filling the computed values held in the FP rotating register, using two non-rotating integer registers to hold the rotating stack memory locations, when there are no FP rotating registers to hold the computed values, where there are no rotating integer registers available, and further when there are only a few non-rotating integer registers available for holding rotating stack memory locations." (emphasis added to show amendments)

Claim 27 is an article version of the claimed method discussed above (claim 21). As discussed above for claim 21, Applicant cannot find **the branch structure** as recited in claim 27. Thus, for at least this reason, Applicant submits that Srinivasan does not teach each and every element as claimed in amended claim 27, thus claim 27 is not anticipated by Srinivasan.

Regarding claim 30:

Amended claim 30 recites:

"A system comprising:
a bus;
a processor coupled to the bus;
a memory coupled to the processor; and
a network interface coupled to the processor and the memory, wherein the processor to spill and fill multiple computed values, in a register, that are live across multiple stages in a software-pipelined loop, by performing:

checking for availability of rotating integer registers and non-rotating integer registers, to spill and fill computed values held in a FP rotating register, that are live across multiple stages in a software-pipelined loop;

spilling and filling the computed values, held in a FP rotating register, using the rotating integer registers to hold [[the]] rotating stack memory locations, when there are no FP rotating registers available to hold the computed values;

spilling and filling the computed values, held in the FP rotating register, using the non-rotating registers to hold the rotating stack memory locations, when there are no FP rotating registers to hold the computed values and further when there are no rotating integer registers available for holding rotating stack memory locations; and

spilling and filling the computed values held in the FP rotating register, using two non-rotating integer registers to hold the rotating stack memory locations, when there are no FP rotating registers to hold the computed values, where there are no rotating integer registers available, and further when there are only a few non-rotating integer registers available for holding rotating stack memory locations." (emphasis added to show amendments)

Claim 30 is a system version of the claimed method discussed above (claim 21). As discussed above for claim 21, Applicant cannot find **the branch structure** as recited in claim 30. Thus, for at least this reason, Applicant submits that Srinivasan does not teach each and every element as claimed in amended claim 30, thus claim 30 is not anticipated by Srinivasan.

Regarding claims 8-9, 12-13, 15, 19-20, 22-25, 28-29, and 31-32

Claims 8-9, 12-13, 15, 19-20, 22-25, 28-29 and 31-32 are dependent claims of independent claims 7, 10, 14, 18, 21, 27 and 30, thus for at least the reasons discussed above for independent claims 7, 10, 14, 18, 21, 27 and 30, dependent claims 8-9, 12-13, 15, 19-20, 22-25, 28-29 and 31-32 are not anticipated by Srinivasan.

Accordingly, Applicant requests respectfully that the Examiner reconsider and withdraw the §102 rejections of claims 7-10, 12-15, 18-25, and 27-32.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 373-6970) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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